IN THE CLAIMS:

1. (Currently Amended) A method of forming at least one field effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of said at least one transistor;

implanting ions of at least one material through the portions of the surface of said substrate not covered by said at least one gate structure by exposing the surface of said substrate to at least one ion beam of said at least one material so as to substantially amorphize the exposed portions of said surface to a predefined depth;

wherein said at least one ion beam is kept at a tilt angle of between 45-80 degrees with respect to a direction perpendicular to said surface of said substrate.

2. (Canceled)

3. (Original) The method of claim 1, wherein said at least one material comprises heavy inert ions.

4. (Original) The method of claim 3, wherein said heavy inert ions comprise one of xenon, germanium, silicon, argon, or a combination thereof.

5. (Original) The method of claim 1, wherein the implanting energy is in the range of approximately 50-150 keV.

6. (Currently Amended) The method of ~~claim 1~~ claim 5, wherein the implanting dose is in the range of approximately $1 \times 10^{11}/cm^2$ to $1 \times 10^{14}/cm^2$.

7. (Currently Amended) The method of claim 1, wherein said semiconductive ~~material~~ substrate comprises one of silicon and germanium.

8. (Original) The method of claim 1, wherein said field effect transistor is one of an NMOS and a PMOS transistor.

9. (Original) The method of claim 1, wherein said substrate is rotated approximately 180 degrees about an axis perpendicular to said surface at least once during implanting.

10. (Currently Amended) A method of forming at least one field effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of said at least one transistor;

implanting ions of at least one first material during a first implantation step through the portions of the surface of said substrate not covered by said gate structure by exposing the surface of said substrate to at least one ion beam of said at least one first material so as to substantially amorphize the exposed portions of said substrate to a predefined depth;

implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of said substrate not covered by said gate

structure so as to form halo structures into the amorphized portions of said substrate;

wherein during said first implantation step said ion beam is kept at a tilt angle of between 45-80 degrees with respect to a direction perpendicular to the surface of said substrate.

11. (Canceled)

12. (Original) The method of claim 10, wherein said at least one first material comprises heavy inert ions.

13. (Original) The method of claim 12, wherein said heavy inert ions comprise one of xenon, germanium, silicon, argon, or a combination thereof.

14. (Original) The method of claim 10, wherein the implanting energy during said first implantation step is kept in the range of approximately 50-150 keV.

15. (Currently Amended) The method of ~~claim 10~~ claim 14, wherein the implanting dose during said first implantation step is in the range of approximately $1 \times 10^{11}/\ cm^2$ to $1 \times 10^{14}/\ cm^2$.

16. (Currently Amended) The method of claim 10, wherein said semiconductive ~~material~~ substrate comprises one of silicon and germanium.

17. (Original) The method of claim 10, further comprising implanting ions of a second predefined conductivity type opposed to the first conductivity type during a third implantation step into the amorphized portions of said substrate.

18. (Original) The method of claim 17, further comprising:

forming spacer elements adjacent to a portion of the sidewalls of said gate structure; and

implanting ions of a predefined conductivity type corresponding to one of said first and second conductivity types during a fourth implantation step through at least the portions of said surface not covered by said gate structure and said spacer elements.

19. (Original) The method of claim 10, wherein said field effect transistor is one of an NMOS and a PMOS transistor.

20. (Original) The method of claim 10, wherein said substrate is rotated approximately 180 degrees about an axis substantially perpendicular to said surface at least once during said first implantation step.

21. (Original) A method of forming at least one field effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of said at least one transistor;

implanting ions of at least one material through the portions of the surface of said substrate not covered by said at least one gate structure by exposing the surface of said substrate to at least one ion beam of said at least one material so as to substantially amorphize the exposed portions of said substrate to a predefined depth;

wherein the tilt angle of said ion beam with respect to a direction perpendicular to the surface of said substrate is varied according to a predefined time schedule comprising a plurality of implanting periods, and

wherein said tilt angle is kept within a predefined range during each implanting period.

22. (Original) The method of claim 21, wherein said tilt angle may be varied in the range of approximately 10 to 80 degrees.

23. (Original) The method of claim 21, wherein said at least one material comprises heavy inert ions.

24. (Original) The method of claim 23, wherein said heavy inert ions comprise one of xenon, germanium, silicon, argon, or a combination thereof.

25. (Original) The method of claim 21, wherein said implanting periods have different lengths.

26. (Original) The method of claim 21, wherein said tilt angle is kept substantially constant during each implanting period.

27. (Original) The method of claim 21, wherein the implanting energy is varied according to the predefined time schedule and wherein, during each implanting period, the implanting energy is kept within a predefined range.

28. (Original) The method of claim 27, wherein said implanting energy is varied in the range of approximately 50-150 keV.

29. (Original) The method of claim 21, wherein the implanting dose is varied according to said predefined time schedule and wherein the implanting dose is kept within a predefined range during each implanting period.

30. (Original) The method of claim 29, wherein said implanting dose is varied in the range of approximately $1 \times 10^{11} / \text{cm}^2$ to $1 \times 10^{14} / \text{cm}^2$.

31. (Currently Amended) The method of claim 21, wherein said semiconductive ~~material~~ substrate comprises one of silicon and germanium.

32. (Original) The method of claim 21, wherein said field effect transistor is one of an NMOS and a PMOS transistor.

33. (Original) The method of claim 21, wherein said substrate is rotated approximately 180 degrees about an axis substantially perpendicular to said surface at least once during each implanting period.

34. (Original) A method of forming at least one field-effect transistor on a semiconductive substrate, the method comprising:

forming at least one gate structure above an active region of said at least one transistor;

implanting ions of at least a first material during a first implantation step through the portions of the surface of said substrate not covered by said gate structure by exposing the surface of said substrate to at least one ion beam of said at least one material so as to substantially amorphize the exposed portions of said substrate to a predefined depth;

implanting ions of a first predefined conductivity type during a second implantation step through the portions of the surface of said substrate not covered by said gate structure so as to form halo structures into the amorphized portions of said substrate;

wherein during said first implantation step the tilt angle of said ion beam with respect to a direction perpendicular to the surface of said substrate is varied according to a predefined time schedule comprising a plurality of implanting periods, and

wherein said tilt angle is kept within a predefined range during each implanting period.

35. (Original) The method of claim 34, wherein during said first implantation step said tilt angle may be varied in the range of approximately 10 to 80 degrees.

36. (Original) The method of claim 34, wherein said at least one material comprises heavy inert ions.

37. (Original) The method of claim 36, wherein said heavy inert ions comprise one of xenon, germanium, silicon, argon, or a combination thereof.

38. (Original) The method of claim 34, wherein said implanting periods have different lengths.

39. (Original) The method of claim 34, wherein the tilt angle is substantially kept constant during each implanting period.

40. (Original) The method of claim 34, wherein during said first implantation step the implanting energy is varied according to said predefined time schedule and wherein during each implanting period the implanting energy is kept within a predefined range.

41. (Original) The method of claim 40, wherein said implanting energy may be varied in the range of approximately 50-150 keV.

42. (Original) The method of claim 34, wherein during said first implantation step the implanting dose is varied according to said predefined time schedule and wherein the implanting dose is kept within a predefined range during each implanting period.

43. (Original) The method of claim 42, wherein said implanting dose may be varied in the range of approximately $1 \times 10^{11}/cm^2$ to $1 \times 10^{14} / cm^2$.

44. (Currently Amended) The method of claim 34, wherein said semiconductive ~~material~~ substrate comprises one of silicon and germanium.

45. (Original) The method of claim 34, further comprising implanting ions of a second predefined conductivity type opposed to said first conductivity type during a third implantation step into the amorphized portions of said substrate.

46. (Original) The method of claim 45, further comprising:

forming spacer elements adjacent to a portion of the sidewalls of said gate structure; and

implanting ions of a predefined conductivity type corresponding to one of said first and second conductivity types during a fourth implantation step through at least the portions of said surface not covered by said gate structures and said spacer elements.

47. (Original) The method of claim 34, wherein said field effect transistor is one of an NMOS and a PMOS transistor.

48. (Original) The method of claim 34, wherein during said first implantation step said substrate is rotated approximately 180 degrees about an axis substantially perpendicular to said surface at least once during each implanting period.